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SE-6787

B. E. III (Sem. V) (EC/ECC) Examination

April / May – 2011

Microprocessor Programming and Interfacing

EC 504

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 3 (Sem. 5) (EC/ECC)**

Name of the Subject :

☛ **Microprocessor Programming & Interfacing EC 504**

☛ Subject Code No. : **6 7 8 7** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Attempt all the questions.

(3) Assume suitable data whenever necessary.

(4) Figures to right indicate full marks.

(5) Use of scientific calculator Casio fx 82, 83, 100 of any compusory.

SECTION - I

1 (a) Answer the following in brief : **10**

(i) What do you mean by bus connection ? How is it avoided ?

(ii) What are important features of 8279 chip ?

(iii) State the function of following 8085 pins.
(a) Ready (b) HOLD

(iv) Show the control signals ($\overline{IOR}, \overline{IOW}, \overline{MEMW}, \overline{MEMR}$) generation using 74138 decoder from the control signals available from 8085 chips.

(v) What do you mean by wait state ? When and hot it can be inserted ?

(b) Discuss the internal architecture of 8085 with necessary block diagram. Draw status register and explain it. **5**

2 (a) Draw the complete interfacing diagram to interface : **8**

(i) 2k EPROM

(ii) 2k RAM with 8085.

EPROM address should start to location 0000H and RAM at location 4000H.

(b) Draw and explain timing diagram of instruction XTHL. **7**

OR

(a) Design I/O interfacing to interface two LEDS using common anode and common cathode technique. Design circuit and draw the interface. Write a program to blink them alternately. Assume suitable port address. **8**

(b) Interface 8254 chip having control register address 83H to 8085 microprocessor. Write a program to generate a 1 kHz square wave from counter 1. Assume wave input is 2 MHz and GATE is connected to + 5V. **7**

3 Answer the following : (any **three**) **15**

(a) Write a short note on DMA and DMA controller.

(b) Explain functional block diagram of 8255.

(c) What is key debouncing ? Explain how it can be avoided using hardware and software techniques.

(d) State difference between memory mapped I/O and I/O mapped I/O.

(e) Explain functioning of IC 8279.

SECTION - II

4 (a) Answer the following in brief : **10**

(i) Explain function of call instruction in 8085.

(ii) Explain importance of auxilary carry in 8055.

(iii) Explain the function of RIM.

(iv) List the name of hardware and software intercepts.

(v) What is instruction cycle and machine cycle ?

(b) Draw and explain 8085 general purpose and special purpose registers and status flags. **8**

(c) Explain the function of EI and DI. **2**

5 Attempt any **two** : **16**

(a) Explain following instructions with example :
(i) DAA (ii) LHLD (iii) STAX (iv) CMC

(b) Draw and explain timing diagram of LXI instruction. Assume necessary data.

(c) What are various software intercepts in 8085 and give their locations. Also explain their usefulness.

(d) Explain 8085 vector interrupt in detail.

6 Attempt any **two** : **14**

(i) Write an assembly language program to shift the block of 10 nos. stored at location starting from 2100H onwards to other location starting from 2200H.

(ii) Write an assembly language program to arrange 10 no.s in ascending order.

(iii) Write an assembly language programme for the addition of 2×2 matrix; answer should be stored of location D200H onwards.
